

Fig. 1

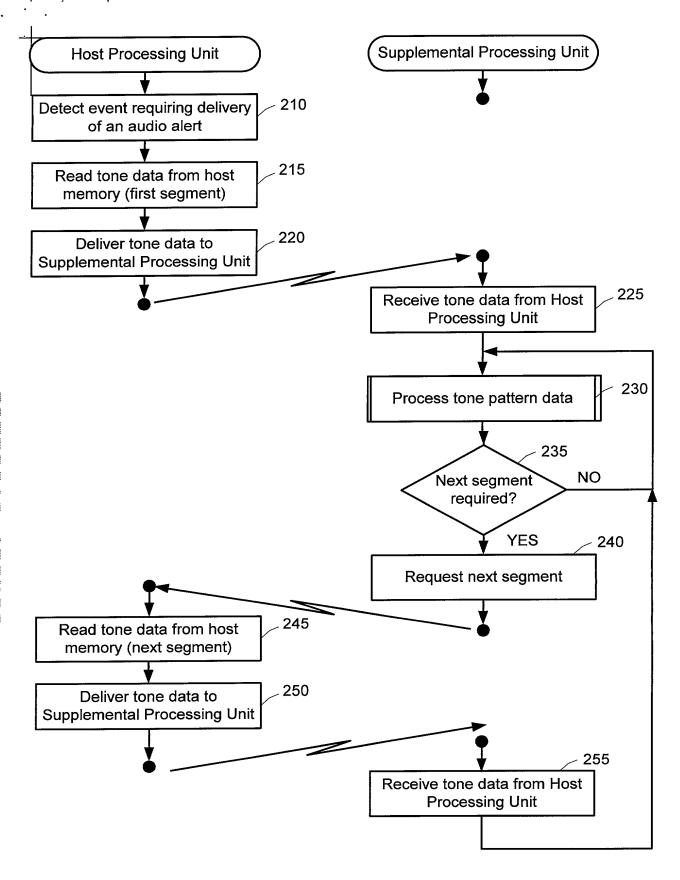


Fig. 2

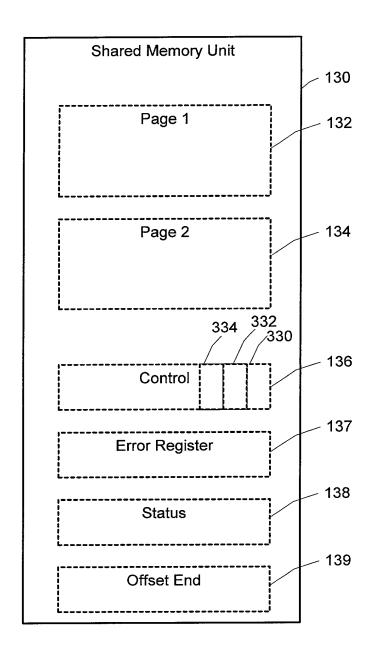


Fig. 3

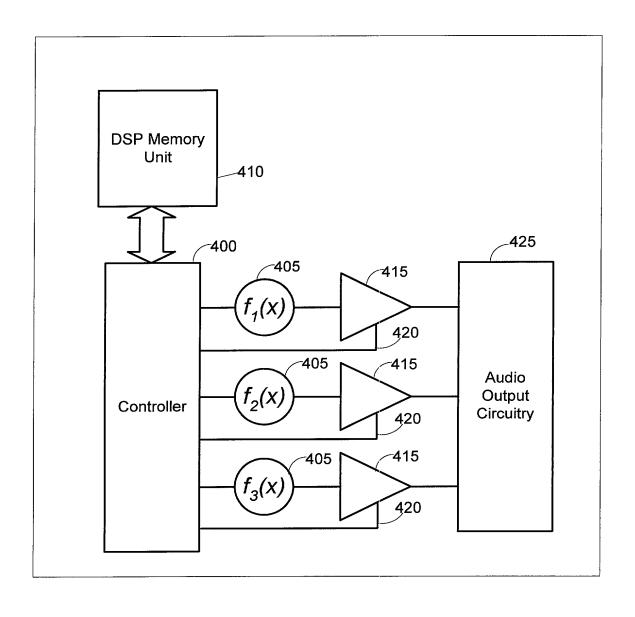


Fig. 4

Data Structure Field	Memory Required (bytes)	Values/Ranges	
Event Number	2	0001-FFFF	
Delta Time	2	Delay in 5msec increments 0000h-FFFFh	502
Track Number	1	1, 2, 3	504
Frequency	2	1-4000Hz	506
Volume	2	0 - off 1-FFFFh	508

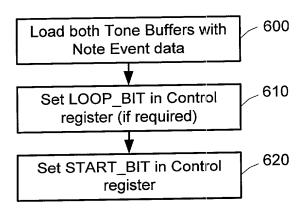
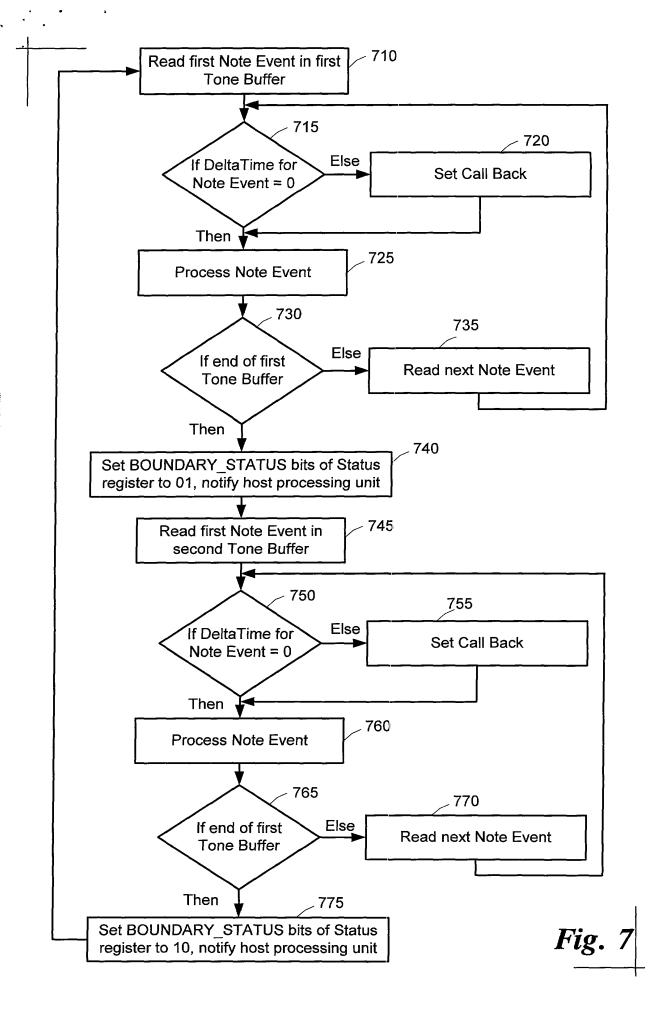


Fig. 6a

Set STOP_BIT in Control register



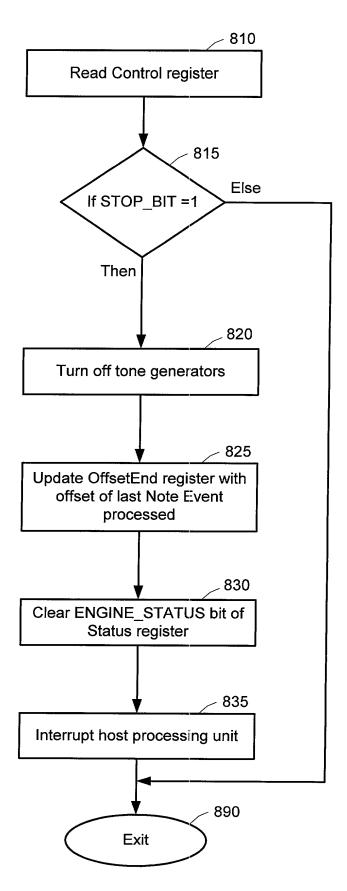


Fig. 8

